DATA SHEET

CREATE: 29 August 2009
REV. NO. 101209

SR9824

24 CHANNEL PARALLEL CORRELATOR CIRCUIT FOR GPS AND GLONASS RECEIVERS

FEATURES

- 24 Fully Independent Correlation Channels
- Switchable to Receive GPS or GLONASS Codes
- Input Multiplexer for Multiple GPS Front-Ends – Allows Antenna Diversity
- Input Multiplexer for GLONASS Multiple (Separate Channels) Front-Ends
- On-Chip Dual UART and Real Time Clock
- Fully Compatible with GP2010/5, and Maxim GPS Receiver Front-End
- Memory and peripheral control logic for AD2106x and ARM micro processors
- 100-pin Plastic Quad Flatpack
- Power Dissipation Less Than 100mW

APPLICATIONS

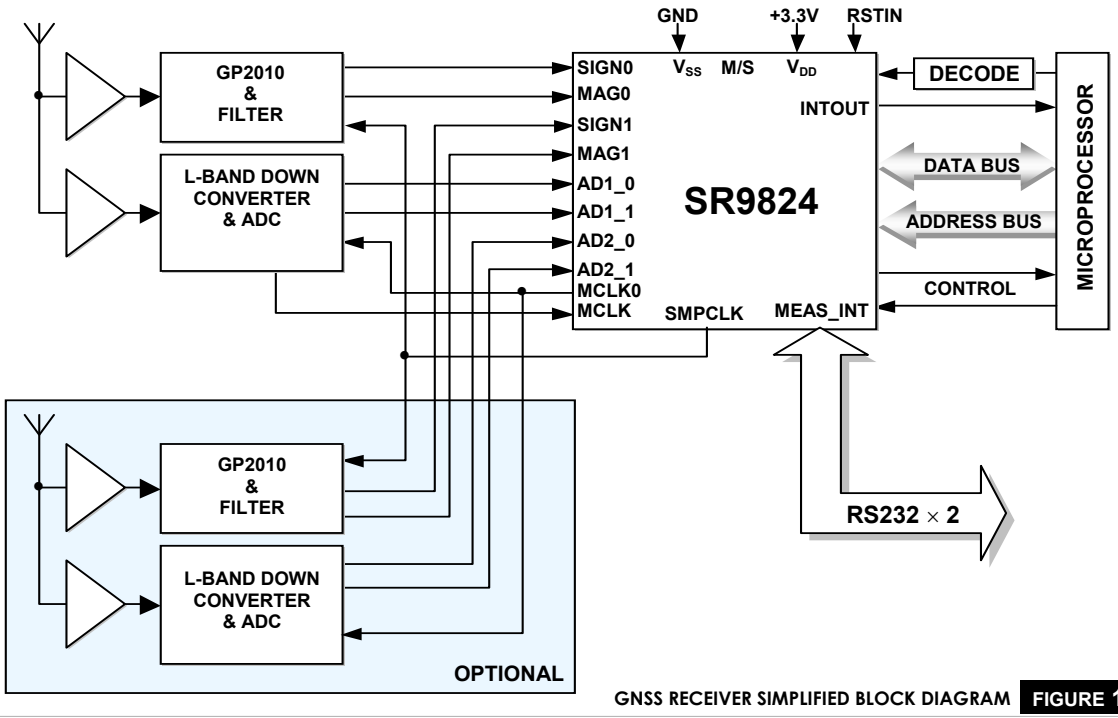
- GNSS Navigation Systems
- High Integrity Combined Receivers
- GNSS Geodetic Receivers
- GNSS Time Reference

TYPICAL GNSS RECEIVER (see Fig. 1)

All GPS satellites use the same L1 frequency of 1575·42MHz, but different Gold codes, so a single front-end may be used.

Each GLONASS satellite will use a different 'L1' carrier frequency, in the range 1598·0625 to 1615·500MHz, with 0·5625MHz spacing, but all with the same 511-bit spreading code, so wide-band receiver used with a single front-end.

To achieve better sky coverage it may be desirable to use more than one antenna, in which case separate front-ends will be needed.



GNSS RECEIVER SIMPLIFIED BLOCK DIAGRAM **FIGURE 1**

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VDD	I/O supply voltage	2.97	3.3	3.63	V
V_{IH}	Input High Voltage	2.0	—	5.5	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
VT	Threshold point	1.45	1.58	1.74	V
VT+	Schmitt trig Low to High threshold point	1.44	1.50	1.56	V
VT-	Schmitt trig. High to Low threshold point	0.89	0.94	0.99	V
I_L	Input Leakage Current	—	—	±10	µA
IOZ	Tri-State output leakage current	—	—	±10	µA
RPU	Pull-up Resistor	39	65	116	kΩ
RPD	Pull-down Resistor	40	56	108	kΩ
V_{OL}	Output low voltage IOL=2,4…24mA	—	—	0.4	V
V_{OH}	Output high voltage IOH=2,4…24mA	2.4	—	—	V
I_{OL}	Low level output current VOL=0.4V 2mA	2.4	4.0	5.0	mA
	4mA	4.7	8.0	10	mA
	8mA	9.4	15.9	19.8	mA
	12mA	14.2	23.9	29.8	mA
	16mA	18.9	31.8	39.8	mA
	24mA	28.3	47.8	59.7	mA
I_{OH}	High level output current VOH=2.4V 2mA	2.8	5.9	9.5	mA
	4mA	5.6	11.9	19	mA
	8mA	11.2	23.8	38.3	mA
	12mA	16.8	35.7	57	mA
	16mA	22	47.7	76	mA
	24mA	33.7	71.5	115	mA

PIN DESCRIPTIONS

NOTE 1. 10µF and 0.01µF ceramic bypass capacitor is required to externally connect between VDDint and GND.

NOTE 2. 4.7µF ceramic bypass capacitor is re-

NOTE 3. The functions of RW and WEN pins depend on whether the GP1020 is in Motorola™ (MOT/INTEL = '1') or Intel™ mode (MOT/INTEL = '0'). In Motorola mode, WEN is an enable (active high) and RW is Read/Write select ('1' = Read). In Intel mode RW is Read, active low, and WEN is Write also active low.

V_{SS}	**3, 13, 34, 42, 43, 50, 58, 100**
V_{DD} (3.3V)	**2, 29, 61, 84**
$V_{DD\ INT}$ (3.3V)	**93**
VREF_1.8 (Output 1.8V)	**94**
GND	**95**

NOTE 4. WRPROG is used to modify the timing of bus operations; when it is held HIGH the internal write signal is ORed with ALE to allow time for the internal address lines to stabilize; when it is held LOW there is no delay added to write.

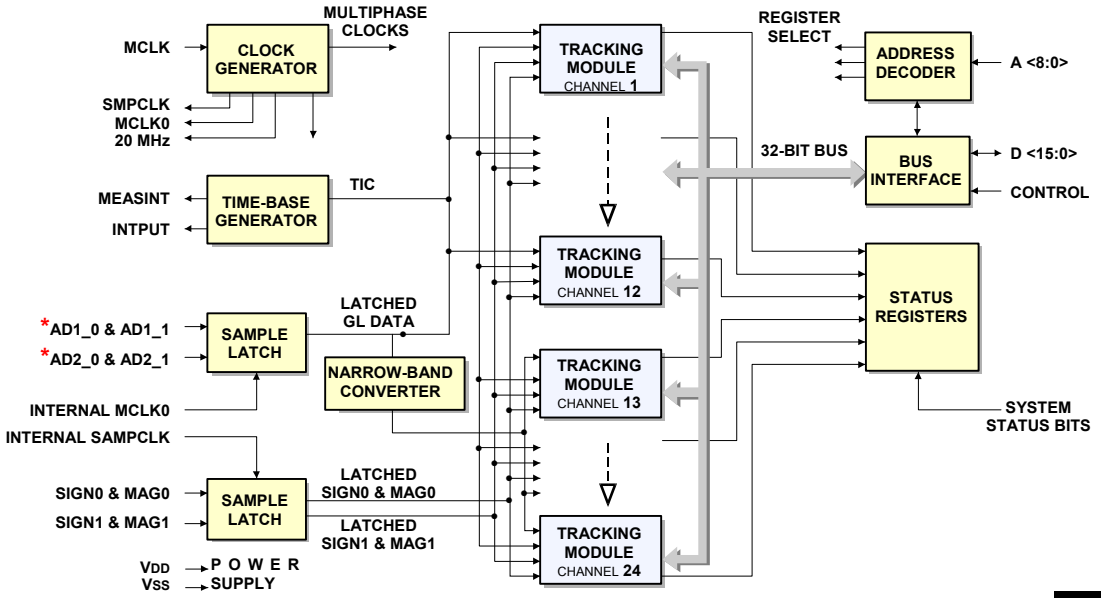
NOTE 5. All **V_{SS}** and all **V_{DD}** pins must be used in order to ensure reliable operation.

Pin Number	Pin Name	Direction/Type	description
1	IED0	IN	External Data Input 0
2	VDDH	POWER	
3	VSSH	GND	
4	ADI2_1	IN	GL SV Input I2_1
5	ADQ2_1	IN	GL SV Input Q2_1
6	ADI2_0	IN	GL SV Input I2_0
7	ADQ2_0	IN	GL SV Input Q2_0
8	ADI1_1	IN	GL SV Input I1_1
9	ADQ1_1	IN	GL SV Input Q1_1
10	ADI1_0	IN	GL SV Input I1_0
11	ADQ1_0	IN	GL SV Input Q1_0
12	CLK40D	IN	40 MHz Clock (UART)
13	VSSC	GND Core	
14	MCLK	IN	40 MHz Master Clock
15	MCLKO	OUT	40 MHz Output
16	PMCLK	IN	Polarity MCLKO
17	SMPCLK	OUT	Sampling clock to down-converter
18	RTCINT	IN	Real time clock interrupt input
19	SIGN1	IN	Satellite Input 1, Sign
20	MAG1	IN	Satellite Input 1, Magnitude
21	SIGN0	IN	Satellite Input 0, Sign
22	MAG0	IN	Satellite Input 0, Magnitude
23	MS1	IN	ROM addr. pre decode strobe
24	MS3	IN	Correlator addr. pre decode strobe
25	MS2	IN	Interfaces addr. pre decode strobe
26	BITECNTL	OUT	BITE control to down-converter GPS
27	PLLLOCKN	IN	PLL lock status from down-converter
28	GLBIT	OUT	BITE control to down-converter GL
29	VDDH	POWER	
30	PLLLOCKG	IN	I/P to monitor GLONASS front-end
31	TMAG	OUT	Test PRN Pattern Magnitude o/p
32	TSIGN	OUT	Test PRN Pattern Sign output
33	TICO	OUT	TIC output from Master
34	VSSH	GND	
35	CDA	IN	To GND
36	RXA	IN	Receive Data input to Channel A of the dual UART
37	TXA	OUT	Transmit Data output from Channel A of the dual UART
38	CTSB	IN	To GND
39	RXB	IN	Receive Data input to Channel B of the dual UART
40	CDB	IN	To GND
41	TXB	OUT	Transmit Data output from Channel B of the dual UART
42	VSSH	GND	
43	VSSC	GND Core	
44	DISCOPN	OUT	On/Off control for LNA by GPS
45	DISCOPG	OUT	On/Off control for LNA by GLONASS
46	TMARK	OUT	One pulse per second output
47	MARKFB	IN	Time Mark line driver feedback
50	VSSH	GND	
51	CSBT	OUT	Boot ROM chip select
52	WRRTC	OUT	Write strobe external RTC
53	RDRTC	OUT	Read strobe external RTC

Pin Number	Pin Name	Direction/Type	description
54	RSTIN	IN	Master Reset (active low)
55	BMS	IN	Boot Memory Select
56	CSRTC	OUT	Chip select external RTC
57	ALERTC	OUT	Address latch enable external RTC
58	VSSH	GND	
59	RESET	OUT	Master Reset (active low)
60	INTOUT	OUT	Interrupt out to microprocessor
61	VDDH	POWER	
63	RD	IN	Bus control – read strobe
64	WR	IN	Bus control – write strobe
66	A9	IN	Register Address, bit 9
67	A8	IN	Register Address, bit 8 (Test mode, GND)
68	A7	IN	Register Address, bit 7
69	A6	IN	Register Address, bit 6
70	A5	IN	Register Address, bit 5
71	A4	IN	Register Address, bit 4
72	A3	IN	Register Address, bit 3
73	A2	IN	Register Address, bit 2
74	A1	IN	Register Address, bit 1
75	A0	IN	Register Address, bit 0
76	D0	INOUT	Data Bus, bit 0
77	D1	INOUT	Data Bus, bit 1
78	D2	INOUT	Data Bus, bit 2
79	D3	INOUT	Data Bus, bit 3
80	D4	INOUT	Data Bus, bit 4
81	D5	INOUT	Data Bus, bit 5
82	D6	INOUT	Data Bus, bit 6
83	D7	INOUT	Data Bus, bit 7
84	VDDH	POWER	
85	D8	INOUT	Data Bus, bit 8
86	D9	INOUT	Data Bus, bit 9
87	D10	INOUT	Data Bus, bit 10
88	D11	INOUT	Data Bus, bit 11
89	D12	INOUT	Data Bus, bit 12
90	D13	INOUT	Data Bus, bit 13
91	D14	INOUT	Data Bus, bit 14
92	D15	INOUT	Data Bus, bit 15
93	VDD_{int}	POWER	
94	VREF_1.8	Core POWER	(Output 1.8V)
95	GND	GND	
96	OED3	OUT	External Data Output 3
97	OED2	OUT	External Data Output 2
98	OED1	OUT	External Data Output 1
99	OED0	OUT	External Data Output 0
100	VSSH	GND	

FUNCTIONAL DESCRIPTION

The SR9824 is a 24-channel digital Correlator which may be used to acquire and track the GPS C/A code or the GLONASS signals. The SR9824 incorporates a 24-channel GNSS Correlator.
The SR9824 has on-chip support for the AD2106x 32-bit processors .
12 channels of the SR9824 includes independent digital GLONASS conversion to narrow-band, independent digital down-conversion to baseband, C/A and GLONASS code generation, correlation, and accumulate-and-dump registers.
Another 12 channels of the SR9824 don't includes independent digital GLONASS conversion to narrow-band.
Fig. 2 shows a block diagram of the Correlator. It consists of the following blocks:



CORRELATOR BLOCK DIAGRAM **FIGURE 2**

SOFTWARE REQUIREMENTS

The very wide variety of types of GNSS receiver needs to operate the correlator in different ways. So to accommodate this and also to allow dynamic adjustment of loop parameters, the SR9824 has been designed to use software for as many functions as possible. This flexibility means that the device cannot be used without a microprocessor closely linked to it, but as a processor is always needed to convert the output of the SR9824 into useful information this is not a significant limitation.

The software associated with the SR9824 can be divided into two separate modules:

1. Acquire and track satellite signals to give pseudo-ranges.
2. Process pseudo-ranges to give the navigation solution and format it in a form suitable for the user.

For the Navigation Solution to be possible all of the pseudoranges must have exactly the same clock error, which can then be removed iteratively to give real ranges if sufficient satellites are tracked (three if the height is known, otherwise four). This need for exact matching of timing errors explains the need for all of the complicated synchronisation between all 12 channels of the correlator.

The following relates only to the signal processing aspects of the software, to acquire and track signals from up to twelve satellites and to obtain the pseudo-ranges and the navigation message. The operation of the navigation software is not dependent on the details of the correlator, and so does not need to be included in this data sheet.

A pair of on-chip interrupt timebase signals are provided to help implement a data transfer protocol between the microprocessor and the 12-channel correlator at fixed time intervals; these signals are:

1. INTOUT - used to interrupt the microprocessor to retrieve accumulated data (1·023ms worth) - period of interrupt normally less than 1ms.
2. MEAS_INT - used to interrupt the microprocessor to retrieve Measurement data that occurs every TIC (approximately 100ms period).

These interrupts can be used to achieve instant response from the microprocessor via an Interrupt Service Routine. Otherwise software based polling scheme will be needed; the choice is set by the application. If the INTOUT interrupt is used, and perhaps also if polling is used, the data transfer rate is about twice the correlation result rate for each channel, so many transfers will not give new data. Examining the status registers before each transfer to see if new data is available and then only reading the data if it is useful can reduce bus use.

The very wide variety of types of GNSS receiver needs to operate the correlator in different ways. So to accommodate this and also to allow dynamic adjustment of loop parameters, the SR9824 has been designed to use software for as many functions as possible. This flexibility means that the device cannot be used without a microprocessor closely linked to it, but as a processor is always needed to convert the output of the SR9824 into useful information this is not a significant limitation.

The software associated with the SR9824 can be divided into two separate modules:

1. Acquire and track satellite signals to give pseudo-ranges.
2. Process pseudo-ranges to give the navigation solution and format it in a form suitable for the user.

For the Navigation Solution to be possible all of the pseudoranges must have exactly the same clock error, which can then be removed iteratively to give real ranges if sufficient satellites are tracked (three if the height is known, otherwise four). This need for exact matching of timing errors explains the need for all of the complicated synchronisation between all 12 channels of the correlator.

The following relates only to the signal processing aspects of the software, to acquire and track signals from up to twelve satellites and to obtain the pseudo-ranges and the navigation message. The operation of the navigation software is not dependent on the details of the correlator, and so does not need to be included in this data sheet.

A pair of on-chip interrupt timebase signals are provided to help implement a data transfer protocol between the microprocessor and the 12-channel correlator at fixed time intervals; these signals are:

1. INTOUT - used to interrupt the microprocessor to retrieve accumulated data (1·023ms worth) - period of interrupt normally less than 1ms.
2. MEAS_INT - used to interrupt the microprocessor to retrieve Measurement data that occurs every TIC (approximately 100ms period).

These interrupts can be used to achieve instant response from the microprocessor via an Interrupt Service Routine. Otherwise software based polling scheme will be needed; the choice is set by the application. If the INTOUT interrupt is used, and perhaps also if polling is used, the data transfer rate is about twice the correlation result rate for each channel, so many transfers will not give new data. Examining the status registers before each transfer to see if new data is available and then only reading the data if it is useful can reduce bus use.

It is important to note that the timing of each of the correlator channels will be locked to its own incoming signal and not to each other or to the microprocessor interrupts, so new data is generated asynchronously. The sampling instant of measurement data of all channels however is common to give a consistent navigation solution.

In order to acquire lock to the satellites as quickly as possible, the data from the last fix should be stored as a starting point for the next fix. It is also useful to make use of the embedded real-time clock on the chip to give a good estimate of GNSS time for the next fix; the navigation solution can be used to measure clock drift and calculate a correction for the clock to overcome ageing. The user's location (or a good estimate of it) along with the Almanac and the correct time will indicate which satellites should be searched for. These may be used to find an estimate of Doppler effects, while the previous clock error is the best available estimate of the present clock error. If this information is not available then the receiver must scan a much wider range of values, which will greatly increase the time to lock. The satellite Clock Correction and Ephemeris are needed for the navigation solution, so if a recent set is held in memory the calculations may begin as soon as lock is achieved and not need to wait for the Satellite Navigation message re-transmission (18 to 36 seconds).

❑

PACKAGE INFORMATION

PLASTIC LQFP-100 PIN